REMARKS

Claims 1-17 remain pending in the application.

No new issues are raised, nor is further search required, as a result of the Amendments made herein. It is therefore respectfully requested that the Amendment be entered.

Claims 1-17 over Frampton, Perets and Feemster

In the Office Action, claims 1-17 stand rejected under 35 U.S.C. §103(a) as allegedly being obvious over U.S. Pat. No. 5,802,351 to Frampton ("Frampton") in view of U.S. Pat. No. 5,537,576 to Perets et al. ("Perets") and further in view of U.S. Pat. No. 5,608,873 to Feemster et al. ("Feemster"). The Applicants respectfully traverse the rejection.

Claims 1-7 recite first and second mailbox portions **both** defined at least in part over **common** memory addresses, the first mailbox addressably filling upward through to a **highest** physical address of the common memory, and the second mailbox addressably filling downward through to a **lowest** physical address of the common memory. Claims 8-17 recite a **contiguous** block of **shared** memory, a first mailbox addressably filling upward through to a **highest** physical address of the **common** memory, and a second mailbox addressably filling downward through to a **lowest** physical address of the **common** memory.

The distinctions of the claims over the THREE references theoretically combined by the Examiner were discussed in detail in the Amendment filed October 7, 2003, and the Examiner provided a response in the Office Action at pages 5-6. The Examiner's Response to Arguments is insightful and helpful.

In the Response to Arguments, the Examiner acknowledges the Applicants' argument that Frampton and Perets disclose separate blocks of memory for the first and second memory banks/mailboxes, and as a consequence the first and second mailboxes are not defined over common memory addresses. In response, the Examiner not only agrees, he acknowledges that he "strongly agrees".

Furthermore, the Examiner and the Applicants are in full agreement that Perets discloses a first memory bank 14 that grows/fills from FFF(hex) towards FE00(hex), and a second memory bank 15 that grows/fills from 0 towards 0CFF(hex).

The ONLY point of disagreement about the theoretical teachings is whether or not the combination of the THREE references teaches the use of **common** memory as recited by claims 1-17.

The Applicants maintain that NONE of the THREE references combined by the Examiner disclose the use of **common** memory as recited by claims 1-17.

The Examiner's position is that "the next logical conclusion" from Perets teaching a first memory bank 14 that grows/fills from FFF(hex) towards FE00(hex), and a second memory bank 15 that grows/fills from 0 towards 0CFF(hex), "is to say that the address space 35 is a common memory address because the first and second memory banks (14 and 15) grow towards each other. Also address space 35 starts from 0 to FFFF, thus "forming a common memory address. (Office Action at 5)

Perets teaches a technique wherein a first 512 byte portion of a 65536 byte memory has a negative offset with respect to a common boundary between first and second banks (See, e.g., Perets, claim 1, and col. 8, lines 41-42; lines 63-65), and another 512 byte portion of that comparatively huge 65536 byte memory has a positive offset. These small bits of memory are lined up at opposite ends of the 65536 byte memory. One intent of this is to be accommodating to expansion such that when it is desired to utilize a 1024 byte memory bank instead of the previous 512 bytes, the latter are simply replaced by new modules. (Perets, col. 8, lines 41-43). These modules are presumably replaced on one end or the other, making one end or the other larger.

The examiner ties this in to the present invention, wherein a complete memory is present at all times, and a mailbox is arranged to flow upwards all the way in memory as necessary, and another mailbox is arranged to flow downwards all the way in memory as necessary. Peret's module expansion technique does not teach mailbox growth or sharing of common memory. In fact,

Perets has no SHARED MEMORY--it has an addressing scheme that adds address from the top and bottom as modules are added. Taking the Examiner's position to the extreme, Perets would somehow be interpreted as teaching the physical piggybacking of modules over same address space. That is, if the physical module expansion technique taught by Perets were applied to the concept of the present invention, modules would be added over ALL memory addresses from the top to the bottom, and another set of modules would be added over ALL memory address from bottom to top. There would be TWO memory spaces at each address--and STILL they would not be common memory as one processor would access one set of the modules, and another processor would access the other set of modules.

Claims 1-17 require defined memory block areas that **OVERLAP**. Moreover, claims 1-17 require **mailbox portions** to be defined in over common memory addresses.

Even the combination of Frampton, Perets and Feemster combined do not result in **mailbox portions** defined over common memory as recited by claims 1-17.

Moreover, the Examiner relies improperly on features that are argued as being inherent in Perets. In particular, the Examiner alleges from the teachings of Peret that the "next logical conclusion is to say that the address space 35 is a common memory address because the first and second memory banks (14 and 15) grow towards each other. Also address space 35 starts from 0 to FFFF, thus a common memory address." (Office Action at 5).

It is respectfully submitted that this is not only wrong, but is purely conjecture on the part of the Examiner in establishing an improper 'inherency' argument.

First of all, under the doctrine of necessary inherency, anticipation may be established when a single prior art reference fails to disclose the claimed invention ipsissimis verbis, but the natural and invariable practice of the reference would necessarily inherently meet all the elements of the claim. See, e.g., Verdegaal Bros., Inc. v. Union Oil Col. of Cal., 814 F.2d 628, 2 USPQ2d 1051 (Fed. Cir. 1987); In re King, 801 F.2d 1324, 231 USPQ 136 (Fed. Cir.

1986); Tyler Refrigeration v. Kysor Indus. Corp., 777 F.2d 687, 227 USPQ 245 (Fed. Cir. 1985); Ethyl Molded Products Co. v. Betts Package Inc., No. 85-111 1032 (D.C.E.D. Kent. 1988). The doctrine of inherency is available only when the inherency can be established as a certainty; probabilities are not sufficient. In re Oelrich, 666 F.2d 578, 581, 212 USPQ 323, 326 (CCPA 1981); In re Chandler, 254 F.2d 396, 117 USPQ 361 (CCPA 1981); Ethyl Molded Prod. Co. at 1032.

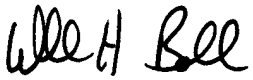
However, the use of **inherency** at all is **entirely improper** with respect to a section 103 rejection, which is the case here. The concept of inherency has no place in determinations of obviousness under section 103, as opposed to anticipation under section 102, because "it confuses anticipation by inherency, i.e., lack of novelty, with obviousness, which, though anticipation is the epitome of obviousness, are separate and distinct concepts." Jones v. Hardy, 727 F.2d 1524, 1529, 220 USPQ 1021, 1025 (Fed. Cir. 1984); See also In re Grasselli, 713 F.2d 731, 739, 218 USPQ 769, 775-76 (Fed. Cir. 1983)

Furthermore, the Examiner's creation of the "next logical conclusion" from Peret's teachings is wrong because the growth towards each other as taught by Perets never comes even close to meeting, much less overlapping to create a common memory address. The disclosed example of Perets uses a 512 byte memory module addressed at either end of a 65,536 byte spacing in memory. The memory doesn't exist between the two modules. Thus, not only does Perets not teach common memory, but the disclosed embodiments don't even HAVE memory between the two memory banks 14 and 15.

Conclusion

All objections and rejections having been addressed, it is respectfully submitted that the subject application is in condition for allowance and a Notice to that effect is earnestly solicited.

Respectfully submitted,



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